



HYPERCHIP
CORE IP SYSTEMS

The PBR-1280 Core IP System *Scalable by Design*

From its inception, Hyperchip architected the PBR-1280 to conveniently address increasing bandwidth and processing requirements within the Point of Presence (PoP). The PBR-1280 also accommodates changes in technology within the installed environment without the need to decommission existing equipment. This criteria forms the basis of selection for Next Generation Networks in order to assure carriers that reasonable operational growth can be re-established and network cost levels can be controlled deterministically.

This document outlines the unique elements of the PBR-1280 with respect to scalability. However, Hyperchip's approach to scalability forced the development of essential features that result in extreme benefits even as related to the smallest, single chassis system available. So by having "Scalability by Design", Hyperchip perfected the following features, which are mandatory for larger systems, yet hugely beneficial for systems of all sizes:

- **System Reliability:** As capacity requirements increase, the core IP system must adhere to true carrier-class reliability and resiliency. The PBR-1280 incorporates full hardware and software redundancy, as well as in-service maintenance, hardware upgrades, capacity increases, and software upgrades.
- **Deterministic QoS:** The primary concern within large systems is addressing possible internal congestion. Hyperchip has unique intra-system protocols (AQUA, SHARE) that allow large systems to avoid internal congestion and deliver deterministic performance per traffic class. These developments, combined with a system-wide QoS-aware scheduling architecture, allow even a single chassis system to deliver ATM-grade quality of service.
- **Distributed Control Processing:** To address the needs of a growing Internet, network elements must be able to scale their control plane. Hyperchip's unique Helix multi-processor approach, combined with the unique distributed software architecture of the HeliOS operating system, allows the PBR-1280 to increase the processing resources available to any protocol, at any time. This assures carriers that as the Internet scales, so can their core IP network.
- **Technology Evolution:** A growing system must have the capability to take advantage of technological developments as they become available. By introducing chassis-to-chassis interconnection based on high-speed parallel optics, service providers are assured that technology change will be integrated with full compatibility. Once installed, a PBR-1280 Core IP System can be augmented in service, with whatever new developments become available (for example, higher density).



Scalability is an essential ingredient for Next Generation Network architectures. Service providers require the assurance that the future of their selected core platform is sound. They require the assurance that they can break the costly "forklift" upgrade cycle every 18 months - that technology provisioned to service today can remain effective for many years to come.

Although the PBR-1280 has been designed for in-service capacity upgrades extending beyond 65,000 ports, the features that such scalability demands are available in single chassis systems – carrier-grade reliability, deterministic QoS, and distributed control processing supporting Logical Routers. Because of these features, a single chassis PBR-1280 system can be the functional equivalent of many traditional routers clustered together, and in addition provide the QoS necessary for network convergence and advanced services and the scalability to expand towards tomorrow’s requirements.

Hyperchip Matrix™ ASIC

The Hyperchip Matrix switch fabric ASIC provides the cornerstone of the PBR-1280’s scalability. The Matrix ASIC is a 16x16 crossbar switch, with dedicated memory and arbiters embedded at each cross-point — a self-scheduling, self-buffering, intelligent crossbar efficiently supporting variable packet lengths. These unique characteristics, when arranged in a Beñes topology and supported by Hyperchip’s internal traffic management algorithms (AQUA, SHARE), enable the PBR-1280 to provide 100% non-blocking performance regardless of system size.

Switch Fabric Architecture

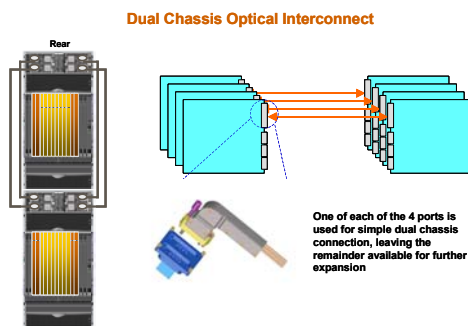
The PBR-1280 uses a quad switching plane architecture. Multi-chassis systems are formed using a Beñes switch fabric topology. Such a topology is not a new development, having been used for many years within telecom circuit switches for its non-blocking attributes. However, efficiently maintaining those attributes when handling “bursty” packet-based traffic creates a challenge. The key to the PBR-1280’s scalability is not only the Matrix, the Beñes topology, the internal traffic management, or the efficient chassis interconnect – it is the unique combination of all of these elements.

Traffic Management

The PBR-1280 traffic management engines maintain 100% non-blocking performance by 1) avoiding internal congestion at any point within the system and 2) avoiding any unnecessary traffic. In order to address these issues, Hyperchip developed AQUA and SHARE. SHARE (SHaping And Resource Equalization protocol) is a backpressure mechanism that originates at each egress port and cascades throughout the switch fabric, addressing any short-term bandwidth and internal congestion issues. AQUA (Adaptive Queue Utilization Algorithm) is a fine-grained feedback mechanism from the egress ports to the ingress. AQUA assures that during congestion, packets that will be dropped due to policies and provisioning are dropped at the ingress port, keeping the switch fabric for only that traffic that will eventually egress the system.

Physical Connectivity

A critical component of the expanding system is the Optical Interface Module (OIM), located on the rear of the system above the switch fabric.



The OIMs, each addressing a single plane of the switch fabric, perform two essential functions:

- Provide optical connectivity between chassis. Each OIM houses VCSEL transceivers that allow for physical chassis dispersion for deployment flexibility.
- Dynamic reconfiguration of Beñes topology as chassis are added. Within each OIM is an electronic crossbar that re-adjusts the Beñes one plane at a time, without user intervention and without any traffic loss.

The PBR-1280 A New Era in IP Networking

The PBR-1280 is the basis for a revolution in the way architects and planners see the progression of telecommunications. It allows for a carrier-grade approach to data networking, reduces the number of diverse networks, simplifies PoP operations, and allows for cost effective expandability to address planned and unforeseen needs well into the future. The PBR-1280 is the solution for Next Generation Networking.