

## Hyperchip Inc. Patent Log

	Description	Pat. No.	Status	Priority Date	Serial No.	Patent Agent	Agency Ref. No.	Comment
	<b>PBR Logical Routers</b>							This covers the fundamental FIB combiner essential for efficient logical routers with single-pass forwarding.
1.1	Forwarding System with multiple logical sub-systems		Pending	2002-11-20	US 10/299,857	SB	P(US)2002-109 86655-22	The U.S. patent office has acknowledged that Hyperchip was first to invent, but Chiaro was first to file in the U.S. Hyperchip has not been able to find enough in its archives to sustain first-to-invent over first to file, and so will drop this in the U.S. at the next office action. Fortunately Chiaro's U.S. patent is so narrow that it does not block Hyperchip from using logical routers in the U.S..
1.3	China	ZL200380103743.1	Issued	2002-11-20	200380103743	SB	P(CN)2002-109 86655-27	Hyperchip filed first in China, so this has been examined and issued in full.
1.4	Japan		Pending	2002-11-20	2004-552298	SB	P(JP)2002-109 86655-31	Hyperchip filed first in Japan, so on examination this is expected to issue in full.
1.5	Korea		Pending	2002-11-20	10-2005-7009100	SB	P(KO)2002-109 86655-29	Hyperchip filed first in Korea, so on examination this is expected to issue in full.
1.6	Europe		Pending	2002-11-20	3773387.0	SB	P(EP)2002-109 86655-30	Chiaro filed first in Europe, so this will be dropped in Europe.
	Logical Router Extensions (in drafting)		Drafting					Hyperchip has made numerous improvements to Logical Routers since the first patent application, covering ACLs, Statistics, MPLS, etc, and is drafting an application to file in the U.S., and then Europe to have all practical Logical Router implementations covered in the U.S. and Europe as well as the fundamental coverage already in place in China and pending in Korea and Japan.
	<b>PBR Traffic Management</b>							Traffic Management is the key to Quality-of-Service, and Hyperchip's traffic Management has been called the 'World's best IP QoS' (NTT) and the only first-rate router QoS (BT), with low latency and jitter even under severe congestion. AQUA (Adaptive Queue Utilization Algorithm) is the heart of Hyperchip's QoS (hence the international filings). SHARE (SHaping And Resource Equalization) is an internal adjunct to AQUA.
2.1	Method and system for congestion avoidance for packet switching devices (AQUA)		Pending	2001-09-27	US 09/963,487	SB	P(US)2001-041 86655-15	This is the only patent application that Hyperchip has ever resorted to appeal on (the appeal brief has been submitted). The U.S. Examiner doesn't recognize the difference between measuring bandwidth (bits per second), and averaging measurements of queue depth (bits). Since the Examiner's position contradicts mathematics, and since the AQUA patents have already been examined and issued in both China and Europe, Hyperchip expects the appeal in the U.S. to be successful.
2.2	Method and system for congestion avoidance for packet switching devices (China)	ZL 02819147.1	Issued	2001-09-27	02819147	SB	P(CN)2004-004 86655-12	Issued
2.3	Europe	EP 1430642	Issued	2001-09-27	2762191.1	SB	P(EP)2004-005 86655-13	Issued, and validated in Germany, France, and the U.K.
3	Congestion management for packet routers (SHARE)	US 7,215,639	Issued	2007-05-08	US 09/943,004	SB	P(US)2001-102 86655-1	Share is a fast adjunct to AQUA that maintains QoS within switch fabrics.
	<b>PBR Switch Fabric (Matrix,OIM)</b>							Since Hyperchip does not plan to use these patents in future products, Hyperchip has sold this group of patents (with yellow highlight) to Intellectual Ventures for U.S. \$1.5 million. Hyperchip retains the right to use these patents in any and all products, and a one-time right to sell that right to use. Since Intellectual Ventures approached Hyperchip, some large company (e.g. Cisco, IBM, Ericsson, Huawei, Alcatel, etc.) must be using these patents, but Hyperchip does not know which one(s). In any case, the remaining right to these patents could be used defensively (the right-to-use would trump any infringement suit), but not offensively (a purchaser could not sue others for infringement).
7.1	Cell-based switch fabric architecture implemented on a single chip	US 6,990,096 B2	Issued	2001-06-01	US 09/870,766	SB	P(US)2001-044 86655-2	Patents 7-11 are for the Matrix chip at the heart of Hyperchip's PBR-1280 (original scalable router) switch fabric. Each Matrix chip contain distributed arbitration and scheduling to eliminate bottlenecks, allowing multiple matrix chips to be linked to scale a switch fabric to 65,000 high-speed ports. The Matrix chip was the largest 0.18 micron chip IBM had ever done for a third party, but it achieved first-pass success due to its innovative hierarchical structure and massive parallelism. IBM found the matrix ideal for improving their process yields, and so extra matrix chips are available.
7.3	China		Pending	2001-06-01	02814443	SB	P(CN)2003-018 86655-16	Intellectual Ventures has the right to divide this Chinese application to match the five U.S. Matrix patents
8	Cell-based switch fabric with distributed scheduling	US 7,277,429	Issued	2001-06-01	US 09/870,800	SB	P(US)2001-045 86655-3	See #7.1
9	Cell-based switch fabric with distributed arbitration		Pending	2001-06-01	US 11/474,480	SB	P(US)2001-046 86655-23	See #7.1
10	Cell-based switch fabric with inter-cell control for regulating packet flow	US 6,990,097 B2	Issued	2001-06-01	US 09/870,767	SB	P(US)2001-047 86655-20	See #7.1
11	Cell-based switch fabric with control for regulating injection of packets	US 7,197,042	Issued	2001-06-01	US 09/870,841	SB	P(US)2001-048 86655-6	See #7.1
12	Programmable interconnect system for scalable router	US 7,274,702	Issued	2001-11-27	US 09/994,017	SB	P(US)2001-139 86655-21	Hyperchip developed the world's first in-service-scalable router switch fabric. The technology covered by this patent allows that scaling to be done simply by adding new chassis, without ever having to un-cable any current chassis.
	<b>PBR Mechanical</b>							This next group consists of hardware patents that were filed in the U.S. only.
13	Compact shelf unit for electronic equipment rack	US 6,499,609 B2	Issued	2001-06-04	US 09/871,959	OR	P(US)2000-094 17272-1US	Space-saving improvement to fan trays
14	Insertion and extraction aid for printed circuit card	US 6,494,729 B1	Issued	2001-06-04	US 09/871,942	OR	P(US)2000-153 17272-2US	Space-saving compound lever for extracting circuit board from chassis
15	Midplane for data processing apparatus	US 6,608,762 B2	Issued	2001-06-01	US 09/870,842	SB	P(US)2001-068 86655-25	A simple very high performance midplane for chassis that have line card and switch fabric cards perpendicular to each other.
16	Apparatus and method for inspecting optical fiber end face	US 7,239,788	Issued	2003-05-27	US 10/445,315	OR	P(US)2003-002 17272-3US	Electro-Industries / GaugeTech has expressed interested in this patent but has not made a sufficient offer.
17	Circuit breaker module safety device and method	US 6,812,416 B2	Issued	2003-05-29	US 10/447,329	OR	P(US)2003-007 17272-4US	Safety feature that shuts off power if breaker-module door is opened - prevents arcing. GE Fanuc has expressed interested in this patent but has not made a sufficient offer.
	<b>PBR Control Plane</b>							These are patents related to efficiently scaling a control plane, including scaling individual protocols, across multiple processors and memories, and also on efficient redundancy and resiliency for control planes.
18	Storage and processing of routing information	US 7,054,311	Issued	2001-07-27	US 09/916,200	SB	P(US)2001-078 86655-4	This is the fundamental patent on efficiently scaling the route-table manager. The USPTO allowed most but not all of the defensible claims, so Hyperchip accepted those claims and filed a continuation to pursue even broader claims.
18.1	Storage and processing of routing information		Pending	2001-07-28	11/361,970	SB		This is the continuation to #18. It is ongoing, with the most recent response to an Office Action sent Sept. 1 2009
				2001-07-27	US 09/915,332			
19	Scalable router	US 7,403,530	Issued			SB	P(US)2001-079 86655-5	In Hyperchip routers one can pull a control card without any effect on neighboring routers. This patent covers the efficient resiliency and redundancy of the routing protocols, as well as scaling individual protocols across multiple processors and memories.
19.2	Scalable router - Europe	1 444 806	Issued	2004-02-16	2753985.7	SB	P(EP)2004-002 86655-7	This is the European equivalent of #19. It has been validated in Germany, France and the U.K.
20	Executing multiple tasks in a task set	US 7,310,803	Issued	2001-10-19	US 09/981,883	SB	P(US)2001-110 86655-24	Minor (a few claims). Helps the performance of task switching on router control planes.

**26** Total Number of Applications  
(18 Patents Issued) (8 Pending, with two to (1.1 and 1.6) be replaced)