Hyperchip Inc.

Hyperchip FPGA Cores and Architectures

FPGA Cores (also suitable for ASICs)

CAM-related and Forwarding-related:

- Binary HCAM: near-RAM efficiency binary CAM pipelined to one search per cycle and one update per cycle, for internal FPGA RAM or external SRAM or DRAM. Up to 200 million packets per second (MPPS)
- Longest-Prefix Match HCAM (up to 200 MPPS):
  - Pulls ~99% of IPv4 addresses out of TCAM with one RAM access
  - Pulls 99.9% of IPv4 addresses out of TCAM with two RAM accesses.
  - Pulls 96% of IPv6 addresses out of TCAM with three RAM accesses.
- Efficient internal TCAM for FPGAs (Xilinx, Altera). Single cycle search but multi-cycle update. (Up to 200 MPPS)
- Single-pass logical router forwarding that combines multiple forwarding actions defined by separate control planes into a unified action for a single data plane.

Buffer Management-related:

- Buffer management of 40 Gb/s and 100 Gb/s to RLDRAM with only a single control/table RAM, scale to ~10,000 active buffers (queues at any given time that have at least one packet buffered) out of a queue space of 1M queues).
- Buffer management of 40 Gb/s and 100 Gb/s to DDR3 SDRAM with internal FPGA control RAM (scales to ~1000 active buffers out of a queue space of 1M queues).
- Deterministic single-step re-order and reassembly at up to 300 million packet segments per second (up to 50 Gb/s of bandwidth), with single-segment management of an RLDRAM buffer.

QoS-related: (25M, 100M and 250M PPS)

- Egress-to-ingress congestion avoidance for carrier-class QoS (512K queues).
- Traffic Scheduler
- trTCM

Security-related:

- Dynamic filtering of 25 million packets per second (extendable to 200 MPPS) for control-plane protection against DoS attacks on routers.

Other Network Processor related: (25M, 100M and 200M PPS)

- SONet Ethernet and MPLS L2 header decoding.
- L3 IP packet decoding, ACL lookups in TCAM with L4 fields.
- Efficient statistics management for RLDRAM
- NPF interface
- Framer management

Hyperchip currently works with Altera FPGAs (Stratix-IV), and has worked extensively with Xilinx (Virtex-II). Hyperchip has also optimized algorithms for Lattice, Cswitch and Achronix FPGAs.

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Hyperchip Architectures

ATCA/MicroTCA-related:

- 100 Gb/s per slot in ATCA system (uses 10Gb/s backplane signaling)
- Smooth Scaling with per-slot switch-fabric granularity
- In-service hardware upgrades with ATCA
- 60 Gb/s of routing on a single-width AMC card.

PCI-e Related:

- 60 Gb/s of routing on a PCI-e card

Hardware-Programmable Network Processors:

- Ingress and egress Network Processors for 40 Gb/s and 100 Gb/s.

Internal pipeline-related:

- Compact ultra-fast pipeline architecture – efficiently handles packets from multiple sources at one packet per cycle with one level of logic per pipeline stage.
- >99.9% efficient variable-length packet format.
- Resource-efficient packet MUX for FPGAs (Xilinx, Altera, Lattice, Cswitch and Achronix) for up to 1024 sources.
- Custom multi-interface-MAC for managing 24 interfaces and decoding 200 million variable-length segments per second with 8 header types, and accumulating multiple 144-bit blocks for each segment for writing to external memory. Four such cores fit into 10% of a mid-sized FPGA.
- Hyperchip is currently adapting a 10G Ethernet MAC to handle up to twelve 10G Ethernet interfaces ports with a single compact multi-interface MAC.

Hyperchip's core expertise is in efficient algorithms and compact ultra-fast code for FPGAs. While Hyperchip's algorithms are currently oriented toward network processing, the underlying pipeline architecture would be well suited to other fields, such as deep packet inspection, encryption, bio-informatics (e.g., BLAST), or any sort of moderately complex digital processing of high-bandwidth data streams.

Hyperchip's current development platform is an AMC-format card (ATCA/MicroTCA compatible. This H40G card has the following resources available for data-intensive processing:

- Up to 200 Gb/s of SerDes I/O
- Over 1 billion (10^9) 160-bit ternary CAM searches per second for pattern matching
- Over 1.2 billion 72-bit DRAM accesses per second for large table lookups
- Over 60 Gb/s of buffering bandwidth available to a gigabyte of DRAM
- Over 50 Tb/s of internal memory bandwidth
- ~500 18-bit GigaOPS or ~50 DP GigaFLOPS internal DSP resources
- 100K-200K adaptive logic modules (over 10^15 Boolean bit-ops/sec)