



HYPERCHIP  
CORE IP SYSTEMS

## PBR-1280 Core IP System *AQUA™ Assured QoS*

Traditionally, IP networks offer a single, best effort class-of-service. Service providers adopted this network architecture due to the inherent limitations of current core IP routing platforms designed with inadequate QoS features and performance. This limitation forced service providers to drastically overprovision their networks to compensate for the absence of performance controls.

Until today, comparisons between core routing vendors focused on raw processing and forwarding performance, ignoring any QoS features. However, Next Generation Networks alter this mindset. QoS assurance enables increasing network resource efficiency, and provides for the convergence of multiple services (ATM, Frame Relay, Voice) and differentiated IP based service (L2, L3 VPNs, VoIP) onto a common, packet-based, IP/MPLS backbone.



The Hyperchip PBR-1280 core IP system addresses these QoS requirements. The PBR-1280 offers a sophisticated approach to QoS, one that has not yet been seen in IP routing, which is more analogous to that offered on traditional ATM based products.

The PBR-1280 architecture guarantees deterministic performance both in single and fully scaled, multi-chassis configurations. Having such an aggressive specification from the conception of the product has led Hyperchip to develop unique, patent-pending internal protocols that prevent congestion within the switch fabric, and assure deterministic QoS system performance in the event of congestion. These unique, intra-system protocols, coupled with an advanced scheduler and packet-processing engine on each interface card, form the basis for the PBR-1280's class-of-service guarantee characteristics.

### **Multi-Level Queuing**

The system supports 8 queues per port with 8 levels of priority assignable to the individual queues. Highest priority traffic will be assured low latency and bandwidth guarantees through the system in the face of any congestion factors.

### **Classification**

The PBR-1280 utilizes an extensive classification engine to determine treatment of packets. Classification can be performed on IP DSCP, IP Precedence and MPLS EXP bits. In addition, the multi-field classifier can classify and mark traffic based on any field up to and including layer 4 headers. This classification assigns packets for individual treatment from policing, scheduling and congestion avoidance algorithms.

### **Traffic Policing**

Hyperchip has implemented a Two-Rate, Three Color Marking algorithm for the PBR-1280 policing function. For each class of service, two rates can be configured: CIR (committed information rate) and PIR (peak information rate). Each packet entering the policing function will fall into one of three categories of conformance:

- Non-conform      Packet has exceeded PIR
- Partial-conform      Packet is between CIR and PIR
- Conform      Packet has not exceeded CIR

Once a level of conformance is established, 3 possible actions can be taken for each packet:

- Drop
- Transit switched with bits remarked (i.e. IP DSCP, IP PREC, MPLS EXP)
- Transit switch unchanged



HYPERCHIP  
CORE IP SYSTEMS

## **Congestion Management (Scheduling)**

In order to guarantee bandwidth and latency during congestion, the PBR-1280 has implemented a 3-stage scheduling algorithm performed at the egress port.

Priority values ranging from 0-7 may be applied to the egress queues. In this way, priority ranges can be given to cover multiple queues and will lead to direct impact for scheduling packets for transmission. Priorities will be serviced in order with weight given to the bandwidth configurations assigned to each queue. By default, queues are set in descending order starting from the EF queue to the BE queue. The PBR-1280 can explicitly guarantee high priority traffic both in terms of bandwidth and latency performance.

## **Congestion Avoidance (AQUA)**

The most difficult area of class-of-service is congestion avoidance. Today's router implementations depend solely on WRED for this function. Hyperchip has developed a suite of internal traffic management algorithms complementing WRED. They enable the PBR-1280 to provide vastly improved congestion management relative to WRED-only implementations, and because they are internal protocols, they do not introduce network interoperability issues.

Two attributes minimize the effectiveness of WRED-only implementations. First, WRED simply determines congestion by looking at average buffer utilization. Second, dropping will be performed at the point of congestion instead of preventing the formation of a congestion point.

To directly augment the shortcomings of WRED, Hyperchip developed AQUA™ – Adaptive Queue Utilization Algorithm. AQUA utilizes the drop probability curves configured for WRED and the bandwidth configurations for each queue. In order to detect congestion, AQUA calculates the average incoming bandwidth for each queue/drop precedence combination per port. This provides a proactive determination of congestion versus WRED. It also allows AQUA to detect an administrative congestion point as well. AQUA will detect bandwidth utilization that exceeds the configured maximum bandwidth per queue and can make appropriate drop probability calculations.

While this implementation would be an improvement on its own, Hyperchip extends AQUA's effectiveness. Instead of the egress making the dropping decision, the drop probabilities are broadcasted to all ingresses. The ingress performs the dropping decision for each destination. This ensures minimum latency regardless of congestion severity. Fairness among flows is also guaranteed since each ingress port receives the identical drop probability. This distribution guarantees an equal proportional dropping policy for all ingresses.

## **The PBR-1280 A New Era in IP Networking**

The QoS implementations in today's core routers have been proven incapable of guaranteeing performance in terms of bandwidth and latency. Traditional techniques such as WRED produce reactive tendencies in the face of congestion, as its algorithm is based solely on queue depth. Congestion points by definition are created at egress ports where packet drops occur. As systems grow to multi-chassis installations, these problems will become amplified because only portions of the router know about local congestion at any given moment.

AQUA guarantees delivery of all premium services, providing benefits to service providers. By delivering deterministic performance across the IP/MPLS backbone regardless of congestion severity, Hyperchip allows voice, legacy data, and IP services to fully converge onto one common backbone. This common infrastructure yields increased efficiency in terms of both operations and capital without sacrificing service quality.